REMARKS

Applicants have carefully reviewed and considered the Office Action mailed on August 5, 2003, and the references cited therewith.

Claims 1 and 70 are amended; as a result, claims 1-14, 16-17, 19-23, and 70-82 remain pending in this application.

Claim Objections

Claim 1 was objected to because of informality. As suggested by the Examiner, claim 1 is amended to correct this informality. Applicants respectfully submit that the entry of this amendment is therefore appropriate after final.

§103 Rejection of the Claims

Claims 1-14, 16, 17, 19-23, and 70-82 were rejected under 35 USC § 103(a) as being unpatentable over Horiguchi et al. ("A Direct Tunneling Memory (DTM)...") in view of Watanabe (U.S. Patent No. 6,133,601). It is fundamental that in order to sustain and obviousness rejection each and every element of the rejected claims must be taught or suggested in the cited references.

Moreover, any suggested combination of references used for purposes of establishing an obviousness rejection must be compatible with the intended teachings and purposes of the cited references. Here, Applicants again assert that the control gate of the Watanabe reference is not the horizontal gate as recited in Applicant's independent claims. Furthermore, Applicants assert that any proposed combination of Horiguchi and Watanabe used to allegedly achieve Applicants' invention is improper hindsight and renders Watanabe useless for its stated teachings and purposes. Correspondingly, Applicants respectfully submit that the present rejections are improper under 35 U.S.C. § 103(a) and are in error.

More specifically, Watanabe teaches increasing capacitance of a memory device with a structure that includes a control gate and floating gate. The control gate is laterally situated and the floating gate is vertically situated. Interposed between the floating and control gates are a separator that is fused around the perimeter of the floating gate. The Watanabe floating gate includes that separator, and its teachings are specifically directed to this separator. Watanabe

asserts that this separator increases capacitance and does so while preventing capacitance variations between the floating gate and the control gate. This structure and teaching are consistent with each and every embodiment disclosed or suggested by Watanabe.

Conversely, Applicants invention requires no such separator and teaches that its structures promote variations in capacitance between the floating and control gates while maintaining total capacitance at conventional levels. That is, by using the structure of Applicants' invention variations in capacitance between the floating and control gates are purposefully and beneficially achieved. This variation ensures that any voltage applied to the control gate will appear in the floating gate. Thus, less voltage is required to program the devices of Applicants' invention than that is required in Watanabe's devices or conventional devices.

Watanabe's teaches and suggest lateral control gates that are separated from floating gates by an insulation film (separator). That separator and structural arrangement permits Watanabe's devices to realize increased capacitance while simultaneously preventing capacitance variations between the control gates and the floating gates.

Watanabe teaches and suggests that this separator interposed between its lateral control gate and vertical floating gate provides its beneficial capabilities. Moreover, Watanabe teaches that capacitance variation between the control gates and the floating gates is not desirable and that it is important to prevent any such variation. These teachings are in direct contrast to Applicants' invention and teachings where in Applicants' invention the variation in capacitance between their horizontal and vertical gates is purposefully and beneficially achieved based on the structure recited in Applicants' claims.

Applicants' horizontal gate is separate from vertical gates by an intergate dialect and not a unique separator arrangement that is taught and suggested by Watanabe. Accordingly, Applicants continue to respectfully assert that Watanabe does not teach or suggest the horizontal gate arrangement taught in Applicants' independent claims. Moreover, one of ordinary skill in this art would not be motivated after having read Horiguchi and Watanabe to alter the structure of Watanabe in order to achieve Applicants' invention. This is so, because in doing so the teachings and benefits of Watanabe are lost, which is that capacitance variation between floating gates and controls gates should be prevented.

Correspondingly, Applicants respectfully request the Examiner's reconsideration of the claims, withdrawal of the rejections, and allowance of the claims.

CONCLUSION

Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney at (612) 373-6904 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6904

Date Oct. 6, 2003

By Daniel J. Kluth
Daniel J. Kluth
Reg. No. 32,146

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 6 day of October, 2003

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